IN THE CLAIMS:

1. (Currently Amended) A semiconductor device, comprising:

a semiconductor substrate;

a gate formed above the semiconductor substrate, the gate having gate sidewall spacers located along sidewalls thereof;

an isolation region ~~located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions of the isolation region~~ formed over the semiconductor substrate, the isolation region including a first portion formed in the trench and a second post portion formed over the trench, wherein no structural interface exists between the first and second portions of the isolation region;

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate~~, wherein the first portion of one of the source/drain region is self-aligned with at least one of the gate sidewall spacers~~.

2. (Original) The semiconductor device as recited in Claim 1 wherein the isolation region is formed adjacent the semiconductor substrate.

3. (Original) The semiconductor device as recited in Claim 1 wherein the isolation region is not located under a channel region.

4. (Original) The semiconductor device as recited in Claim 1 wherein the isolation region comprises an oxide.

5. (Previously Presented) The semiconductor device as recited in Claim 1 wherein the second portion of the one of the source/drain region comprises polysilicon.

6. (Original) The semiconductor device as recited in Claim 1 wherein the isolation region extends through a transistor tub.

7. (Currently Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation region ~~located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions of the isolation region~~ formed over the semiconductor substrate, the isolation region including a first portion formed in the trench and a second post portion formed over the trench, wherein no structural interface exists between the first and second portions of the isolation region; and

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate~~, wherein the first portion of one of the source/drain region is self-aligned with at least one gate sidewall spacer~~.

8. (Original) The semiconductor device as recited in Claim 7 wherein the isolation region is not located under the channel region.

9. (Original) The semiconductor device as recited in Claim 7 wherein the isolation region comprises an oxide.

10. (Previously Presented) The semiconductor device as recited in Claim 7 wherein the second portion of the one of the source/drain region comprises polysilicon.

11. (Original) The semiconductor device as recited in Claim 7 wherein the isolation region extends through a transistor tub.

12. (Currently Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

an isolation region located adjacent but not extending under the channel region, ~~the isolation region being located within a trench formed in the semiconductor substrate and not extending under the channel region and including a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions of the isolation region~~ the isolation region including a first portion formed in the trench and a second post portion formed over the trench, wherein no structural interface exists between the first and second portions of the isolation region; and

source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region and in contact with the second post portion, but not in the semiconductor substrate~~, wherein the first portion of one of the source/drain region is self-aligned with at least one gate sidewall spacer~~.

13. (Original) The semiconductor device as recited in Claim 12 wherein the isolation region comprises an oxide.

14. (Previously Presented) The semiconductor device as recited in Claim 12 wherein the second portion of the one of the source/drain region comprises polysilicon.

15. (Original) The semiconductor device as recited in Claim 12 wherein the isolation region extends through a transistor tub.

16. (Original) The semiconductor device as recited in Claim 12 wherein the source/drain regions are first source/drain regions of a first transistor, and the semiconductor device further includes second source/drain regions of a second adjacent transistor, wherein the first source/drain regions are isolated from the second source/drain regions by the isolation region.

17. (Currently Amended) A semiconductor device, comprising:

a first transistor located adjacent a second transistor, wherein both the first and second transistors are located over a semiconductor substrate;

an isolation region located between the first and second transistors and within a trench located within the semiconductor substrate, ~~wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions of the isolation region an isolation region~~ the isolation region including a first portion formed in the trench and a second post portion formed over the trench, wherein no structural interface exists between the first and second portions of the isolation region;; and

source/drain regions associated with each of the first and second transistors, each of the source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region and in contact with the second post portion, but not in the semiconductor substrate~~, wherein the first portion of one of the source/drain region is self-aligned with at least one gate sidewall spacer~~.

18. (Original) The semiconductor device as recited in Claim 17 wherein the isolation region comprises an oxide.

19. (Previously Presented) The semiconductor device as recited in Claim 17 wherein the second portion of the one of the source/drain region comprises polysilicon.

20. (Original) The semiconductor device as recited in Claim 17 wherein the isolation region extends through a transistor tub.

21. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

providing a semiconductor substrate;

creating a gate above the semiconductor substrate, the gate having gate sidewall spacers located along sidewalls thereof;

forming an isolation region within a trench located in the semiconductor substrate, ~~wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions of the isolation region an isolation region~~ the isolation region including a first portion formed in the trench and a second post portion formed over the trench, wherein no structural interface exists between the first and second portions of the isolation region;

forming a first portion of one of a source/drain region in the semiconductor substrate and a second portion of the one of the source/drain region on the isolation region and in contact with the second post portion but not in the semiconductor substrate~~, wherein the first portion of one of the source/drain region is self-aligned with at least one of the gate sidewall spacers~~.

22. (Previously Presented) The method as recited in Claim 21 wherein forming an isolation region includes forming an isolation region adjacent to the semiconductor substrate.

23. (Original) The method as recited in Claim 21 wherein forming an isolation region includes forming an isolation region that is not located under a channel region.

24. (Original) The method as recited in Claim 21 wherein forming an isolation region includes forming an oxide isolation region.

25. (Previously Presented) The method as recited in Claim 21 wherein forming a second portion of the one of the source/drain region includes forming a second portion of the one of the source/drain region with polysilicon.

26. (Original) The method as recited in Claim 21 wherein forming an isolation region includes forming an isolation region that extends through a transistor tub.

27. (Currently Amended) An integrated circuit, comprising:

semiconductor devices, including;

a semiconductor substrate;

a gate formed above the semiconductor substrate, the gate having gate sidewall spacers located along sidewalls thereof;

an isolation region located within a trench formed in the semiconductor substrate, ~~wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions of the isolation region~~ the isolation region including a first portion formed in the trench and a second post portion formed over the trench, wherein no structural interface exists between the first and second portions of the isolation region;

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate~~, wherein the first portion of one of the source/drain region is self-aligned with at least one of the gate sidewall spacers~~; and

interconnect structures contacting the semiconductor devices.

28. (Original) The integrated circuit as recited in Claim 27 wherein the isolation region is formed adjacent the semiconductor substrate.

29. (Original) The integrated circuit as recited in Claim 27 wherein the isolation region is not located under a channel region.

30. (Original) The integrated circuit as recited in Claim 27 wherein the isolation region comprises an oxide.

31. (Previously Presented) The integrated circuit as recited in Claim 27 wherein the second portion of the one of the source/drain region comprises polysilicon.

32. (Original) The integrated circuit as recited in Claim 27 wherein the isolation region extends through a transistor tub.

Claim 33 (Canceled)